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***PIN Detector Apparatus and Method of Fabrication***

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# PIN DETECTOR APPARATUS AND METHOD OF FABRICATION

## 1. Technical Field

[0001] The present invention relates generally to a method of fabricating PIN (p-type/intrinsic/n-type) detectors and the apparatus produced from the method. More particularly, the present invention relates to a PIN detector that is produced on a substrate having a particular thickness and at a predetermined point during the fabrication process, removing selected portions of the substrate.

## 2. Background

[0002] Conventional thin silicon PIN detectors are typically fabricated from a bulk wafer, *i.e.*, a wafer having a thickness dimension between approximately 150-200 microns. On a front surface of the wafer, detectors are fabricated using semiconductor lithographic and thinfilm techniques. The backside of the wafer is implanted to form the second field plate of the detector. These wafers are then diced and hybridized onto individual readout integrated circuits (ROICs). A wirebond contact is made to the implanted field plate or detector common.

[0003] Prior attempts to process thin PIN detectors include, for example, processing the PIN detector as a thick wafer, for example 150-200 microns, and then mechanically thinning and implanting components at the detector level.

[0004] One conventional semiconductor device of silicon-on-insulator (SOI) complementary metal-oxide semiconductor (CMOS) is disclosed in U.S. Patent No. 5,137,837, entitled, "Radiation-Hard, High-Voltage Semiconductive Device Structure Fabricated on SOI Substrate", issued August 11, 1992 to Chen-Chi P. Chang et al. This semiconductor device includes highly-doped buried n-type and p-type wells in a first silicon layer, which covers an insulator, and over which a second silicon layer is formed with congruent lightly-doped n-type and p-type layers in which complementary MOSFET active devices are formed. While the semiconductor device formed by this process has many advantages, one drawback is that two separate silicon formation steps are required.

[0005] Another conventional CMOS device is disclosed in U.S. Patent No. 5,807,771, entitled, "Radiation-Hard, Low Power, Submicron CMOS on a SOI Substrate", issued September 15, 1998 to Truc Q. Vu et al. This patent relates to a radiation-hard, low-power semiconductor device of the CMOS type that is fabricated with a sub-micron feature size on a silicon-on-insulator (SOI) substrate. The SOI substrate may be of several different types.

[0006] Yet another conventional detector device is disclosed in U.S. Patent No. 4,782,028, entitled, "Process Methodology for Two-Sided Fabrication of Devices on Thinned Silicon" issued November 1, 1998 to Michael G. Farrier et al. This patent relates to a method for forming a detector device, such as a thinned bulk silicon blocked impurity transducer infrared detector, by thinning a semiconductor substrate and processing the thinned region on two sides to form the detector device. The semiconductor substrate is thinned to form a cavity in the substrate. Further processing on both sides of the thinned region is performed while the thinned region is still connected to the thicker substrate. The thinned region is then separated from the substrate upon completion of the processing steps. The device is then mounted to a readout device.

## SUMMARY

[0007] The present invention provides advances in the state of the art by providing an improved PIN detector and method for manufacturing the improved PIN detector. This improved PIN detector and method of fabrication is accomplished by using a substrate, having a full or standard thickness. A field plate is implanted or embedded in an active wafer layer, which is typically between approximately 5 and 200 microns. A contact to the field plate is achieved, such as through a chemically selective, isotropic, or RIE (reactive ion etching) etch that intersects the field plate implant at the buried etch stop. After the detector is hybridized, a portion of the substrate, referred to as the handle portion, can be removed or detached such as with wafer grinding, chemical mechanical polish, a silicon etch (*e.g.*, TMAH or KOH), or a combination of all the above to the BOX (buried oxide). Then the BOX is removed (*e.g.*, via a buffer oxide etchant (BOE) or a dilute HF solution) leaving a thinned PIN

that is typically between approximately 5 and 200 microns thick. Preferably, the entire handle portion and the entire wafer portion are removed. Most preferably, the entire handle portion is removed in one process step. As used herein, one process step includes multiple repetitions of the same process type. For example, removing a portion of a layer by fast etching with a concentrated etchant followed by removing a separate portion of the same layer by slow etching with a dilute etchant constitutes a single process step of removal by etching.

[0008] Accordingly, one embodiment of the present invention is directed to a PIN apparatus that includes a wafer portion, electrical circuitry disposed on a first surface of the wafer portion and a bonding portion disposed on a second surface of the wafer portion. The wafer portion and the bonding portion are portions of a substrate. The substrate is formed by conventional wafer bonding techniques for bonding the wafer portion to a handle portion of the substrate, and disposing an oxide portion therebetween.

[0009] A further embodiment of the present invention is directed to the PIN apparatus described above wherein the thickness of the wafer portion is a function of a minimum thickness of the apparatus.

[0010] Another embodiment of the present invention is directed to a method for fabricating a PIN apparatus. The method includes forming electrical circuitry on a wafer portion of a substrate, the substrate having a handle portion, an oxide material portion, a bonding material portion and the wafer portion. The entire handle portion and the oxide material portion are removed to expose the bonding material portion when the forming process is substantially complete.

[0011] Yet another embodiment of the present invention is directed to a computer operating system stored on a computer-readable medium for directing a computer to execute a method that includes forming electrical circuitry on a wafer portion of a substrate. The substrate having a handle portion, an oxide material portion, a bonding material portion and the wafer portion. The entire handle portion and the oxide material portion are removed to expose at least part of the bonding material portion.

[0012] Yet another embodiment of the present invention is directed to the computer operating system stored on a computer-readable medium described above that further includes establishing a location on the substrate for the removing step to occur.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Various advantages of the present invention will become apparent to those skilled in the art by reading the following specification and by reference to the drawings in which:

[0014] Figures 1-19 are cross-sectional views of the detector device during various steps in the fabrication process.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] The present invention provides advances in the state of the art by providing an improved method for manufacturing PIN detectors. This improved PIN detector and method of fabrication is accomplished by using a substrate, having a full or standard thickness. A field plate is implanted or embedded in the active wafer layer, which is typically between approximately 5 and 200 microns thick. A contact to the field plate is achieved through a chemically selective, isotropic, RIE (reactive ion etch) or DRIE (deep reactive ion etch) silicon etch that intersects the field plate implant at the buried etch stop. After the detector is hybridized, a portion of the substrate, referred to as the handle portion, can be removed or detached with wafer backside grinding, chemical mechanical polishing, silicon etch (*e.g.*, TMAH or KOH), or combination to the BOX (buried oxide) portion. Then the BOX portion is removed (*e.g.*, BOE) leaving a thinned PIN that is typically between approximately 5 and 200 microns thick. Preferably, the thickness of the thinned PIN is less than 100 microns, and most preferably is less than 50 microns. An advantage to the present invention is that the device may be handled as a full thickness substrate and detector chip until the handle wafer portion and etch stop and/or bonding layer are removed. Removal reveals a completed device that has an integrated and reliable field plate connection.

[0016] Another advantage of the present invention is that it eliminates a traditional wirebond connection to the detector common field plate over the thin silicon PIN detectors.

[0017] As will be seen by reading the following text, the present invention results in a more cost effective detector since material costs are reduced. Furthermore, labor costs are reduced since the labor associated with the processing is reduced, particularly thinning of the detector. Furthermore, since the substrate is relatively thick and robust during most of the fabrication process, wafer breakage is substantially reduced. Also the detectors produced by the present method are easier to handle since the substrate portion provides a substantial backing material. Higher output volumes are possible since field plate implantation occurs at the wafer-level. Quality and reliability are improved since the integrated field plate connection is eliminated following the hybridization wirebond. The total thickness variation (TTV) in the detector layer is precisely controlled and not substantially affected by flatness of the ROIC, hybridization results, or the thinning process. Furthermore, thicker substrates permit hybridization of larger FPAs.

[0018] Figure 1 shows a cross-sectional view of a substrate 10 that includes: a handle wafer portion 208, which may be an n-type material such as formed by a Czochralski process (CZ) or a magnetic field applied CZ process (MCZ); a buried oxide layer 206; a buried backside contact portion 204; and an active wafer portion 202. The buried backside contact portion 204 may, for example, comprise arsenic or antimony or phosphorous or other suitable n-type material and may be approximately between 0.01 and 5 microns thick. The intrinsic active wafer portion 202 may be between approximately 5 and 200 microns thick and may be formed by a float zone growth method process (FZ). As used herein the term portion means a separate part or any fraction of the whole, including the entire whole.

[0019] Figure 2 shows a cross-sectional view of substrate 20 that also has oxide layers and photoresist layers. Substrate 20 is similar to substrate 10 described above (*i.e.*, handle wafer portion 208, buried oxide layer portion 206, buried backside contact portion 204, and active wafer portion 202) and further includes oxidation layers 210 and 214 and photoresist layers 212 and 216.

[0020] Oxidation layer 214 is formed on a lower surface of handle wafer portion 208 and oxidation layer 210 is formed on an upper surface of active wafer portion 202. Each oxidation layer 210, 214 is preferably between approximately 2500 Angstroms and 6000 Angstroms thick, nominally between approximately 2900 Angstroms and 3600 Angstroms. The oxide thickness depends on the thickness of layer 202.The oxidation layers 210 and 214 typically comprise $SiO_2$ (silicon dioxide, also referred to as silicon oxide herein) which may be formed, for example, from a wet oxidation process at 925 degrees Celsius.

[0021] Layers 212 and 216 comprise photoresist material, and each layer 212, 216 has a nominal thickness of approximately 1.6 micrometers. Photoresist layer 212 is formed on oxidized layer 210 and photoresist layer 216 is formed on oxidized layer 214. The photoresist material 212 is developed to expose the silicon dioxide that will be removed to allow the substrate 202 to be exposed etch at region 211.

[0022] Figure 3 shows a substrate 30, which is similar to substrate 20 except that substrate 30 shows that photoresist layers 212 and 216, shown in Figure 2, have been stripped. A BOE etch may be used to etch the oxide layer 210, at region 211, such that oxide layer 210 has a nominal target thickness of approximately 3200 Angstroms. Region 211 also illustrates that the oxide layer 210 has been etched to expose a section of active wafer portion 202. Oxide layer 214 is typically not etched. The elements described in relation to Figures 1 and 2 are not discussed in relation to Figure 3 (*i.e.*, handle wafer portion 208, buried oxide layer portion 206, buried backside contact portion 204, and active wafer portion 202).

[0023] Figure 4 shows device 40, which results from further processing substrate 30 shown in Figure 3. (The term device is used to define the substrate 10, which has additional processing performed on it.) Device 40 shows that active wafer portion 202 is etched to expose a portion 207 of the buried oxide layer 206. A region of the buried backside contact portion 204 is etched. One etching compound that may be used is, for example, a KOH (potassium hydroxide) anisotropic etch or plasma oxide etch; however, any suitable etching substance could be used. Surfaces 220(a) and

220(b) are formed, as shown in Figure 4. The other elements have been described previously and are not discussed in relation to Figure 4.

[0024] Figure 5 shows device 50, which results from further processing device 40 shown in Figure 4. Device 50 shows that surfaces 220(a) and 220(b), which were formed from etching active wafer portion 202 and buried backside contact portion 204, are implanted to form layers 222(a) and 222(b). These layers are typically formed using ion implantation of As in a concentration sufficient to make electrical contact to layer 204, the buried backside contact. The other elements have been described previously and are not discussed in relation to Figure 5.

[0025] Figure 6 shows device 60, which results from further processing device 50 shown in Figure 5. Device 60 shows that a photoresist material is applied on surface 210 and layer 222(a) and 222(b) and exposed region of buried oxide layer 206. The photoresist material is stripped to expose the individual detectors of an array, leaving photoresist portion 226(a) on a portion of oxide layer 210, layers 222(a) and 222(b) and exposed region of buried oxide layer 206. Photoresist portions 226(b) and 226(c) remain on another portion of oxide layer 210. The other elements have been described previously and are not discussed in relation to Figure 6.

[0026] Figure 7 shows device 70, which results from further processing device 60 shown in Figure 6. Device 70 shows that oxide layer 210 is etched to form oxide portions 210(a), 210(b), 210(c) and 210(d). Detector areas 230(a) and 230(b), for example to be used as diode detectors, are exposed on the active wafer portion 202. The etching process may be accomplished using a suitable etching compound to remove desired portions so as to form detector areas 230(a) and 230(b). One example is to implant boron to form the detector at sites 230(a) and 230(b). While boron has been used as one example, other P-type dopant materials such as aluminum or gallium may also be used.

[0027] As shown in Figure 7, oxidation layer 214 has been removed from the lower surface of handle wafer portion 208 during the same etch used to expose the detector areas 230(a) and 230(b). The other elements have been described previously and are not discussed in relation to Figure 7.

[0028] Figure 8 shows device 80, which results from further processing device 70 shown in Figure 7. Device 80 shows that photoresist portions 226(a)-(c) are stripped using a suitable stripping compound. An oxide layer 234 is grown on the upper surface of oxide portions 210(a)-(d), implanted surfaces 222(a) and 222(b) and detector areas 230(a) and 230(b). Oxide layer 234 is preferably approximately between 350 Angstroms and 650 Angstroms thick and more preferably approximately 500 Angstroms thick. Oxide layer 234 may be grown, for example, at approximately 1000 degrees Celsius and may be silicon dioxide ($SiO_2$) or other suitable material that exhibits similar characteristics. The oxide layer 234 may also serve as activation anneal for the implanted arsenic and/or boron materials noted above.

[0029] As shown in Figure 8, the oxide layer 234 is not grown on the exposed portion 207 of buried oxide layer 206. The other elements have been described previously and are not discussed in relation to Figure 8.

[0030] Figure 9 shows device 90, which results from further processing device 80 shown in Figure 8. Device 90 shows that a photoresist layer is applied and selectively stripped to form photoresist areas 236(a)-(d) on corresponding portions of the oxide layer 234(a)-(d), respectively. Photoresist layer (generally 236) is, for example, a detector contact implant photoresist.

[0031] Also, as shown in Figure 9, portions of the oxide layer 234 have been etched to expose, for example, the surfaces 222(a) and 222(b) and selected portions of the detector areas 230(a) and 230(b). This step patterns contact openings for the backside contact portion 204 and the detector areas 230(a) and 230(b). The other elements have been described previously and are not discussed in relation to Figure 9.

[0032] Figure 10 shows device 100, which results from further processing device 90 shown in Figure 9. Device 100 shows that the photoresist portions 236(a)-(d) are stripped and a conductive layer 238 is applied to the oxide layer portions 234(a)-(d) and surfaces 222(a) and 222(b) and detector areas 230(a) and 230(b). Conductive layer 238 is, for example, a metal, such as aluminum, copper, silver, platinum, or other electrically conductive material. Layer 238 may be applied, for example, using

a sputtering technique, or other suitable deposition technique, and typically results in a deposition layer between approximately 3500 Angstroms and 6500 Angstroms thick and preferably approximately 5000 Angstroms thick. The other elements have been described previously and are not discussed in relation to Figure 10.

[0033] Figure 11 shows device 110, which results from further processing device 100 shown in Figure 10. Device 110 shows that a photoresist material 240 is applied on an upper surface of layer 238. The photoresist layer 240 is used for metal delineation. The other elements have been described previously and are not discussed in relation to Figure 11.

[0034] Figure 12 shows device 120, which results from further processing device 110 shown in Figure 11. Device 120 shows that selected portions of photoresist layer 240 are removed leaving portions 240(a)-(d) and selected portions of conductive layer 238 are removed leaving portions 238(a)-(d). This processing step also exposes portions of oxide layer 234, *i.e.*, 234(b), 234(c) and 234(d); however, other portions of oxide layer 234(b), 234(c) and 234(d) may not be entirely exposed. As shown in Figure 12, some areas of layer 234 are covered by portions of layer 238 and 240. Any wet or dry aluminum etch technique can generally be used. Additionally, the field plate 204 can be used to control the surface and prevent inversion between the detector areas 230(a) and 230(b) by imposing additional mask and etch steps similar to those above, preferably with an additional ion implantation into the substrate 202. These additional steps may alternatively be performed after formation of the devices but prior to removal of the handle wafer portion 208, followed by annealing with a laser or other heat-focused device.

[0035] Figure 13 shows device 130, which results from further processing device 120 shown in Figure 12. Device 130 shows that photoresist layer 240 has been removed, using a stripping compound, and an oxide layer 242 is applied. Oxide layer 242 is typically, for example, a silicon-based oxide, such as silicon oxide, and applied by a suitable deposition technique at between approximately 400 and 450 degrees Celsius. Oxide layer 242 is applied to cover conductive layer portions 238(a)-(d) and oxide layer portions 234(b)-(d). The other elements have been described previously and are not further discussed in relation to Figure 13.

[0036] Figure 14 shows device 140, which results from further processing device 130 shown in Figure 13. Figure 14 shows that contacts, on device 140, to active device elements 230(a), 230(b), 222(a) and 222(b) are exposed for electrical interconnect, such as indium bump contacts. This may be accomplished by applying a photoresist material 244, and selectively etching the oxide layer 242 and selectively stripping the photoresist material 244 to form bump contact portions 244(a)-(d) on corresponding oxide layer portions 242(a)-(d), respectively. The etching also exposes conductive layer portions 238(a), 238(b) and 238(d). The other elements have been described previously and are not further discussed in relation to Figure 14.

[0037] Figure 15 shows device 150, which results from further processing device 140 shown in Figure 14. Device 150 shows that photoresist material 244 is stripped and a double layer of bump photoresist material 246, such as indium, is applied to form the photoresist portions 246(a)-(d). The other elements have been described previously and are not discussed in relation to Figure 15.

[0038] Figure 16 shows device 160, which results from further processing device 150 shown in Figure 15. Device 160 shows that the bump formations are achieved by depositing a bump metallization and then removing the bump photoresist material 246 to reveal bump formations 248(a)-(c). The formations 248(a)-(c) are in physical contact with corresponding portions of metal layer 238(a), 238(b) and 238(d). The other elements have been described previously and are not discussed in relation to Figure 16.

[0039] Figure 17 shows device 170, which is an inverted device 160 shown in Figure 16. Device 170 shows that the handle wafer portion 208 is positioned so that it may be removed without substantially affecting the relationship or integrity of the other components that are disposed on device 170.

[0040] Figure 18 shows device 180, which results from further processing device 170 shown in Figure 17. Device 180 shows that the handle wafer portion (previously shown herein as element 208), which provided desirable stability and facilitated

handling during the fabrication process, has been removed. Removal of the handle wafer portion may be achieved by silicon etch such as TMAH or KOH or WBG.

[0041] Figure 19 shows device 190, which results from further processing device 180 shown in Figure 18. Device 190 shows that the buried oxide layer (previously shown herein as element 206) has been removed to expose backside contact portion 204. During silicon etches used to fabricate the devices on the active wafer portion 202, the silicon etch may form grooves that develop into holes through the active wafer portion and through the field plate 204. Upon removal of the BOX layer 206 as depicted in Figure 19, some of those holes are then exposed. Generally, the device 190 is secured to a read out integrated circuit ROIC or other supporting substrate with an epoxy selected to prevent the BOE from attacking any metal or underlying circuitry within the device 190. The size of these holes may generally be controlled by the particulars of the etching process, which results in controlling the size of the etch grooves. The etch to remove the BOX layer 206 is preferably done in two process sub-steps as a combination of BOE and PAE etchant. PAE etchant does not attack the underlying metal, and may be used as a pad etch to expose metal contacts through the overglass or conformal coating.

[0042] Figure 19 shows a cross-sectional view of an improved PIN device 190 fabricated according to the present invention. The device 190 has the advantage that a backside contact 204 and oxide portion (shown herein as element 206) are embedded between an active wafer portion 202 and a handle wafer portion (shown herein as element 208) to form the substrate (shown generally herein as element 10). Electrical circuitry is formed on an upper surface of the active wafer portion 202 and upon completion of the formation process, the handle wafer portion (shown herein as element 208) and buried oxide portion (shown herein as element 206) are removed to expose the contact portion 204. This fabrication process permits the handle wafer portion to provide enhanced stability during the fabrication process.

[0043] Thus, the description describes PIN detector fabrication on a substrate. The electrical circuitry is disposed, (*i.e.*, mounted, fabricated) and when the disposition is substantially complete, such that additional processing can be satisfactorily performed on a thinned substrate (*i.e.*, a substrate in which the handle portion and oxide portion

have been removed), the handle portion and oxide portion are removed. The manner in which these portions are removed can either be multiple etching or detaching steps, or a single step to remove both the handle and the oxide portion.

[0044] The removal process for the handle portion is typically a function of the location of the oxide layer and similarly, the removal of the oxide layer is typically a function of the location of the contact layer. The contact layer may be positioned such that the removal of the handle and the oxide portions are based on a pre-determined quantity or, alternatively, the removal may be specific for each particular apparatus.

[0045] It is also an embodiment of the present invention that the fabrication and removal processes can be stored on an electronic medium, such as RAM (random access memory) ROM (read only memory) or other non-volatile memory (NVM). Thus a computer may be used to implement the present invention.

[0046] While the present invention has been described as a series of discrete steps, it is also an embodiment that one or more of the steps described herein could be combined to reduce the number of steps. Also, the disclosed sequence of steps is not critical and it is contemplated that one skilled in the art would be aware of modifications in the sequence of steps described herein. Combining steps and modifying the sequence of the steps described does not depart from the scope of the invention.

[0047] Furthermore, while the present invention has been described in terms of particular materials there are other materials, which may interchangeable, that should be understood by one skilled in the art to be equivalents. Indeed the present invention may be accomplished with any combination of materials that result in a similar result.

[0048] Furthermore, while specific dimensions have been provided to describe the invention, it is contemplated that one of ordinary skill in the art may modify the dimensions without departing from the invention.